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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	09/325,882	
	Filing Date	June 4, 1999	
	First Named Inventor	Sinclair et al.	
	Group Art Unit	2182	
	Examiner Name	Harold Kim	
Total Number of Pages in This Submission	8	Attorney Docket Number	0100.9900390

ENCLOSURES (check all that apply)		
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## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Christopher J. Reckamp Reg. No. 34,414
Signature	
Date	August 6, 2002

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Sinclair et al.  
Serial No. 09/325,882  
Filing Date: June 4, 1999  
Confirmation No. 3412

Examiner: Harold Kim  
Art Group: 2182  
Our file no. 00100.99.0039  
Docket No. 0100.9900390

AUG 14 2002

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Title: **POWER REDUCTION CIRCUIT AND METHOD WITH MULTI CLOCK  
BRANCH CONTROL**

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*Rosalie Swanson*  
Rosalie Swanson

**RESPONSE AFTER FINAL**

Dear Sir:

In response to the final office action mailed May 24, 2002, Applicants respectfully submit the following remarks.

**REMARKS**

Applicants respectfully traverse and request reconsideration and withdrawal of the Final Action. The final Office Action rejects Claims 1-16 based on new grounds of rejection.

Claims 1-3 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,781,768 (Jones Jr.) in view of U.S. Patent No. 6,307,281 (Houston). Jones is directed to a graphics controller utilizing a variable frequency memory clock that is controlled to vary the operation of a frame buffer. The graphics controller includes a plurality of different clock pulse generators and a clock controller (Cora PLL) which selects the clock frequency for a memory clock to a frame buffer memory based on the state of graphics controller functional units. As taught by Jones, the memory clock which is coupled to the frame buffer memory is varied such that the bandwidth of the information from the memory to the graphics processor is